

# Automatic Test Vector Generation for Mixed-Signal Circuits

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## Abstract

*Mixed circuit testing is known to be a very difficult task. This is due to the difficulty of: testing the analog part of the circuit, controlling the digital signal from the analog outputs, observing the analog outputs in the digital circuit, controlling the analog circuit from the digital outputs and observing the digital signals in the analog circuit. As a solution to these problems, we propose an automatic test vector generation for mixed circuits to perform functional testing. In this paper, a case of an analog block followed by a digital block is considered. The experimental results (simulation and discrete realization) show the efficiency of the automatic test generation technique.*

## 1. Introduction

Recent improvements in fabrication technology have made possible the realization of reliable integrated circuits (ICs) containing both analog and digital functions on the same silicon chip. The problem of testing these circuits is, however, much more complicated than that of testing purely digital or analog ICs. The testing demands for each type of circuit are somewhat different. Digital circuit testing, very crudely, consists in checking that the pattern of 1's and 0's at the outputs corresponds to the pattern expected. Analog testing consists in measuring, for example, gain, bandwidth, distortion, impedance, noise, etc. So, different techniques have evolved for the two types of circuits which are difficult to integrate into a single testing solution.

Because the problems mentioned above are difficult to handle, generically specific solutions for standard mixed circuits such as CODECs [1], ISDN [2] and A/D converters [3] have been proposed. The other alternative is the use of Design For Testability (DFT) rules, that basically partition the mixed circuit into analog and digital sections so that the input and output signals of each section can be accessed. One possible implementation of this technique is the use of some analog and digital multiplexers for controllability/observability purposes [4] and [5]. A possible implementation is the use of the mixed-signal test bus standard IEEE P1149.4 [6]. Using this method, both chip area and the number of I/O pins will have to increase to accommodate the test requirements.

Alaa et al.[7] presented a steady-state-response test generation method for mixed-signal integrated circuits. This technique considers catastrophic faults only. Also, the circuit should be modified before being tested by this technique.

In this paper, a new test method for mixed-signal ICs is presented. The circuit is considered as an entity, so there is no need for circuit partitioning into analog and digital blocks. The proposed test generation technique consists of functional testing for the analog parts and test vector generation with constraints for the digital parts. This technique allows the test of every block under the conditions imposed by the other blocks.

For purpose of consistency only the case of *analog-digital* circuits is considered, Figure 1. Other configuration type of a mixed circuit is the subject of another paper.

The rest of the paper is organized as follows: in section 2, the testing procedures for the analog circuit is first reviewed. The test vector generation with constraints (for digital circuit) and fault propagation from one block to another are then presented. Some experimental results are discussed in section 3. A conclusion is given in Section 4.

## 2. Analog-digital circuit testing

Testing a mixed-signal circuit means finding out if the circuit meets some of its specifications. So, the problem of mixed-signal testing is to convert the parameter specifications from the analog domain to the digital domain.

In order to propose a test strategy for a mixed circuit, a testing technique for every block of the circuit is needed. The element testing technique will be used for analog circuits [8]. For the digital circuit an automatic test vector generation technique based on BDD and boolean difference will be used as described in [10].

To test an *analog-digital* circuit, Figure 1, the digital block should be tested under the conditions imposed by the analog block. The effect of a faulty element in the analog block should be propagated through the digital block. The analog part of the A/D converter is considered as a part of the analog block and the digital part is considered as a part of the digital block. For the digital block, the constraints imposed by the analog and conversion blocks are taken into account in the testing procedure.

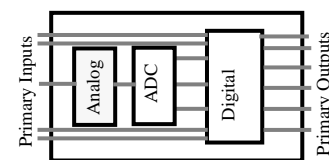


Figure 1: Analog-digital circuit

### 2.1 Test method for analog circuits

Faults in analog circuits can be categorized as catastrophic or parametric (soft). Catastrophic faults are open and short circuits caused by sudden and large variations in components [9]. Parametric or soft faults are defined by the circuit's functionality. In analog circuits, the concern is which parameters to select for testing and the accuracy to which they should be tested in order to detect the variations in the faulty components.

We know that the circuit's parameters depend on the circuit's elements, and finding a test set for the elements of the circuit consists in finding a set of parameters to be measured that guarantees maximum fault coverage of the elements. The maximum fault coverage of an element is defined as the minimum element deviation that can be observed by measuring one parameter. The element coverage is defined as the minimum element deviation that can be observed at one primary output parameter at least. To quantify the coverage of an element, we should compute the relative deviation of the faulty

When considered alone, the digital circuit of Figure 3 is found to be fully testable, which means that 100% coverage

can be obtained. But, when it is a part of the mixed circuit, the fault coverage will change. The dependency introduced by the analog part have an effect on the fault coverage of the digital block. For this circuit, we have found that 2 of the 18 uncollapsed single stuck-at faults considered become undetectable when both circuits are connected. Note that the faults *l0* s-a-1 and *l3* s-a-1 cannot be tested, since lines *l0* and *l1* cannot be controlled to 0 and 0 respectively.

### 2.3 Analog fault activation

If we apply a signal in the analog primary input, all the PIs of the digital part controlled by this analog input will have a logic value equal to 0 or to 1. Suppose that we have to generate test vectors for the analog parts of the mixed circuit in Figure 4. In this circuit, we have supposed that we have only one analog input. Suppose that we have a faulty component in the analog part of the mixed circuit. In other words, the element deviates from its specification tolerance. To activate the fault, the parameter from which the element should be tested is chosen. In order to propagate the fault through the conversion block, the signal to be applied in the analog primary input must force at least one output of the A/D converter to have a different value in the fault-free circuit and in the faulty one. Suppose that a parameter is considered faulty, due to an element deviation, when its deviation exceeds 5%. The analog input should be chosen such that we have an output of the A/D converter that has different values when the parameter deviation is inside the tolerance box  $[-5\%, 5\%]$  and when it is outside the tolerance box.

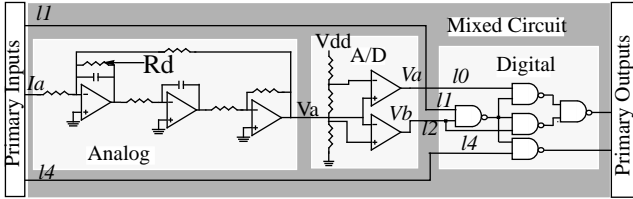


Figure 4: Mixed-signal circuit

To test any element/parameter of the analog circuit, the amplitude  $A$  and the frequency  $f$  must be chosen appropriately. The circuit of Figure 5 will be used as a vehicle to introduce the test vector approach. To activate a fault, we must have different logic values at the output  $V_d$  of a comparator of the conversion block. Table 1 gives, for each parameter to test, the corresponding amplitude and frequency of the signal which should be applied to the analog circuit. The techniques for choosing the amplitudes and frequencies (depending on the cut-off frequencies of the analog circuit) are described in [8].

To test a parameter  $T$  deviation ( $\frac{\Delta T}{T}$ ), two vectors are needed, one to test the upper bound of a parameter deviation and the other to test the lower bound, Table 1.

A parameter  $T$  is considered fault-free if its deviation is inside the tolerance box  $[-x, +x]$  ( $\frac{\Delta T}{T} \in [-x, +x]$ ), otherwise it is faulty. Table 2 gives the notation of the used parameters.

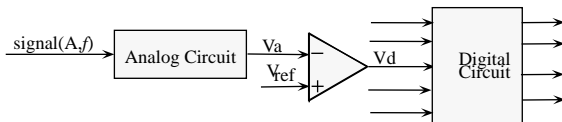


Figure 5: Analog-digital circuit

Table 1: Test set of an analog circuit parameters

Parm. (T)	Test	Input signal		$\frac{\Delta T}{T} < -x$ (faulty)		$-x < \frac{\Delta T}{T}$ (fault-free)		$\frac{\Delta T}{T} > x$ (faulty)		cmp. val.
		f	A	Va	Vd	Va	Vd	Va	Vd	
$A_{DC}$	$A_{DC} > (1+x) \cdot A_{DCn}$	0	$\frac{V_{ref}}{(1+x)A_n}$	$< V_{ref}$	0	$< V_{ref}$	0	$> V_{ref}$	1	$\bar{D}$
	$A_{DC} < (1-x) \cdot A_{DCn}$	0	$\frac{V_{ref}}{(1-x)A_n}$	$< V_{ref}$	0	$> V_{ref}$	1	$> V_{ref}$	1	D
$A_{AC}$	$A_{AC} > (1+x) \cdot A_{ACn}$	$f > 0$	$\frac{V_{ref}}{(1+x)A_f}$	$< V_{ref}$	0	$< V_{ref}$	0	$> V_{ref}$	1	$\bar{D}$
	$A_{AC} < (1-x) \cdot A_{ACn}$	$f > 0$	$\frac{V_{ref}}{(1-x)A_f}$	$< V_{ref}$	0	$> V_{ref}$	1	$> V_{ref}$	1	D
$f_{lcf}$	$f_{lcf} > (1+x) \cdot f_{lcfn}$	$f_{lcfn}$	$\frac{V_{ref}}{(1-y)A_{f_{lcfn}}}$	$> V_{ref}$	1	$> V_{ref}$	1	$< V_{ref}$	0	D
	$f_{lcf} < (1-x) \cdot f_{lcfn}$	$f_{lcfn}$	$\frac{V_{ref}}{(1+y)A_{f_{lcfn}}}$	$> V_{ref}$	1	$< V_{ref}$	0	$< V_{ref}$	0	$\bar{D}$
$f_{hcf}$	$f_{hcf} > (1+x) \cdot f_{hcfn}$	$f_{hcfn}$	$\frac{V_{ref}}{(1+y)A_{f_{hcfn}}}$	$< V_{ref}$	0	$< V_{ref}$	1	$> V_{ref}$	1	$\bar{D}$
	$f_{hcf} < (1-x) \cdot f_{hcfn}$	$f_{hcfn}$	$\frac{V_{ref}}{(1+y)A_{f_{hcfn}}}$	$< V_{ref}$	0	$< V_{ref}$	1	$> V_{ref}$	1	D

Let us explain, for example, how to test a deviation on the parameter  $f_{lcf}$  (cut-off frequency of a low pass filter) of the analog circuit. Suppose that  $f_{lcf}$  deviates from the nominal value by more than  $x\%$ . Suppose also that a deviation of  $x\%$  in the frequency causes a deviation of  $y\%$  in the gain of the analog circuit. In this case, according to Table 1, the amplitude  $B$  and the frequency  $f$  of the analog signal to be applied are respectively  $\frac{V_{ref}}{(1-y)A_{f_{lcfn}}}$  and  $f_{lcfn}$ . Since we have a

low-pass filter, when  $f$  exceeds its nominal value by more than  $x\%$ ,  $A_f$  would decrease by more than  $y\%$ . In other words, when  $f > (1+x)f_{lcfn}$ ,  $A_f < (1-y)A_{f_{lcfn}}$ . In this case,  $V_a = A_f \cdot B \sin(2\pi f)$  is always less than  $V_{ref}$ . In the other case,  $V_a$  is greater than  $V_{ref}$  in a period of time  $T_p$ .  $T_p$  depends on the nominal frequency and its deviation. Then we will have *composite* logic values. In this case, the logic value of the digital circuit lines can be 0, 1, D,  $\bar{D}$ , or equals a boolean function. Note that D is supposed to be a primary input which is last in the BDD ordering.

To propagate the fault, we simply traverse the circuit beginning from the lines at which the logic value is D or  $\bar{D}$  to the POs of the mixed circuit. We compute the OBDD for each line traversed. If this OBDD does not contain the node D, the fault cannot be propagated through this line, so we try another line. In the opposite case, we continue our traversal until we reach a PO. If the OBDD generated contains D, the fault can be

tested, and a test vector is generated by simply choosing a path in the OBDD leading to D.

**Table 2:** Notation of the used parameters

$A_{AC}$	AC gain of the analog circuit
$A_f$	nominal AC gain of the analog circuit
$A_{DC}$	AC gain of the analog circuit when the frequency of the signal is f
$A_{DCn}$	DC gain of the analog circuit
$f_{lcf}$	nominal DC gain of the analog circuit
$f_{lcfn}$	cut-off frequency of a low-pass filter
$f_{hcf}$	nominal cut-off frequency of a low-pass filter
$f_{hcfn}$	AC gain corresponding to the frequency $f_{lcfn}$
$A_{f_{lcfn}}$	cut-off frequency of a high-pass filter
$f_{hcf}$	nominal cut-off frequency of a high-pass filter
$f_{hcfn}$	AC gain corresponding to the frequency $f_{hcfn}$
$A_{f_{hcfn}}$	The deviation seen in the gain, when the frequency deviates by x% from its nominal value
y	a voltage reference from the conversion block
$V_{ref}$	

Then, as in the digital circuit, a fault in the analog part can only be tested if two conditions are satisfied: 1) The fault is activated, and, 2) The fault is propagated to a primary output. Let us take the circuit in Figure 4. This circuit is composed of three sub-circuits:

- 1) Analog sub-circuit, a second order filter that have one input  $Ia$  and one output  $Vd$  connected to the input of the A/D converter.
- 2) An A/D converter whose two outputs are connected to the inputs  $I0$  and  $I2$  of the digital circuit.
- 3) The digital circuit which has two external primary inputs,  $I1$  and  $I4$ , and two other inputs,  $I0$  and  $I2$ , which are connected to the outputs of the A/D converter.

Suppose now that we are interested in testing the deviation of a parameter in the analog block. To test such a fault, we need to activate the fault: force a change in the behavior of at least one of the A/D converter outputs. We need also to propagate the error. Then, an appropriate assignment to the primary inputs  $I1$  and  $I4$  must be chosen in order that we have D or  $\bar{D}$  in at least at one of the primary outputs.

Suppose that the element  $Rd$  of the second order band-pass filter, Figure 4, is faulty. According to equation 2, a deviation in  $Rd$  of less than 9.9% cannot be tested. When the faulty element deviation is greater or equal to 9.9%, this fault can be tested by measuring the amplification gain  $A1$ . So if the  $A1$  deviation exceeds 5% then the fault can be observed at the output of the analog circuit, otherwise it cannot. To test whether or not  $A1$  deviation is inside its tolerance box  $[-5\%, 5\%]$ , the upper and lower bounds of the box should be tested. The first alternative is to observe the fault effect at the output of the comparator  $Co1$ , Figure 4. Then, a sine wave having a frequency of 10khz and an amplitude  $B$  should be applied at the analog input of the mixed circuit.  $B$  should be chosen in order that the amplitude of  $Vd$  is greater than or equal to  $V_{i2}$ , when the deviation is greater than or equal to -5%, and when the faulty element forces  $A1$  to decrease from its nominal value by more than 5%,  $Vd$  will be less than  $V_{i2}$ . Consequently, we have to choose  $B = \frac{V_{i2}}{0.95A1}$  will force  $Vb$  to

switch from 1 to 0. So, in the fault-free case  $Vb$  is 1 and in the faulty case it is 0, which means that in the line  $I2$  of the digital circuit we will have a composite value equal to D. The same thing will be done in order to test the upper bound of  $A1$  except

that  $B = \frac{V_{i2}}{1.05A1}$ . So, in line  $I2$  of the digital circuit, we will have  $\bar{D}$ .

In order to find an assignment to the input lines  $I1$  and  $I4$ , we first generate the OBDD of the output  $Vo1$  with  $I0=D$  and  $I2=\bar{D}$  and we check whatever or not there exists a node corresponding to D in this OBDD. If there does, the fault can be propagated to this output. Otherwise, we generate the OBDD of one of the other outputs.

The OBDDs of  $Vo1$  and  $Vo2$  constructed with  $I0=D$  and  $I2=\bar{D}$  are represented in Figure 6. Note that we can propagate the fault at either of the two outputs, since in the corresponding OBDDs we have a node D. Then, when we set  $I1=1$ , the fault is propagated to  $Vo1$ , and when we set  $I1=1$  and  $I4=1$ , the fault is propagated to both outputs  $Vo1$  and  $Vo2$ .

propagation of the error caused by the analog fault to an output of the mixed circuit.

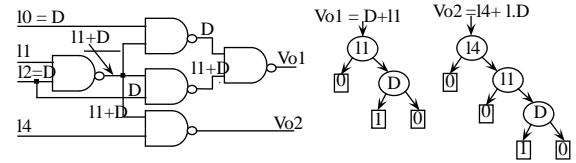


Figure 6: Propagation procedures

The automation of the proposed test vector generation is possible. To obtain a test vector for an element of an analog circuit, the following procedure is used. First, for each element, the parameter that is the most sensitive to a deviation in the element is taken. Using Table 1, we find an analog signal that will activate the fault. In other words, we choose an amplitude and a frequency that sets D or  $\bar{D}$  at one of the primary outputs of the conversion block. When “all the possibilities are studied”, in other words, when all the cases that allow to have D or  $\bar{D}$  at one of the primary outputs of the conversion block has been tried, and the fault cannot be propagated through the digital block, it is impossible to test the fault by measuring the deviation induced on  $T$ . Then, we look for another parameter from the parameter set ( $\{T\}$ ) of  $x_i$ . When all the parameters of the element  $x_i$  have been studied without success, any deviation in this element cannot be seen at any primary output of the mixed circuit. Here, we have supposed that all the POs of the mixed circuit come from the digital block.

### 3. Experimental results

In order to show the effectiveness of the proposed test generation technique, the results are given for two examples: the first one is presented in Figure 4. The second example is composed of a fifth order low-pass chebyshev filter, a conversion circuit made of 15 comparators and 16 resistors, and a digital circuit, one of the ISCAS85 benchmark circuit [11].

Test vectors are generated for the mixed circuit of Figure 4. In case 1, the analog, digital and conversion blocks are considered separately. Thus, we have a direct access to PIs and POs of every block.

As shown in example 2, in order to have the best coverage of all the elements in the analog circuit, when single fault is considered, the parameters  $A1$  and  $A2$  have to be tested. If the parameter deviation is less than 5% then the element error is less than the computed element deviation (E.D). We have found that the same E.D can be tested for the analog circuit in case 1 and case 2. The A/D conversion testing is similar to the analog testing since we propose to test the elements ( $Rc1$ ,  $Rc2$ ,  $Rc3$ ) of the circuit by measuring the voltage references

(vt1,vt2). The element deviation (E.D.) found is the same in case 1 and case 2.

The digital circuit is fully testable when it is considered alone. But when the digital block is a part of the mixed circuit, the number of undetected faults (NUF) is 2. Two faults became untestable due to the constraints imposed by the analog block.

### Example 3

In this example, the analog block is a fifth-order-chebychev filter, the conversion circuit is a comparison circuit made of 15 comparators and 16 resistors. The output of the filter feeds the comparators and the 15 outputs of the comparators are directly related to digital circuit inputs. Since the digital circuit may have more than 15 inputs, the selection of the digital inputs, that are controlled by the comparators, is performed randomly. With this conversion circuit, the digital circuit became more difficult to test because of the constraints imposed by the comparators. For the digital block, some ISCAS85 benchmark circuits are considered [11].

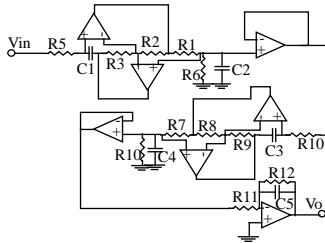


Figure 7: fifth-order-chebychev filter

In case 1, we consider the circuit to be tested is the analog block (Chebychev filter, Figure 7). In this case we have access to the POs and PIs of the analog circuit. In case 2, the analog block is a part of the mixed-signal circuit. In this case, the PI of the analog circuit is the only access point to the circuit, and the analog circuit output should be observed at the digital POs.

Table 3: Test results for the fifth-order-chebychev filter.

Case 1 (Analog block alone)			Case 2 (Analog block is a part of the mixed-signal circuit)		
T	E	ED[%]	T	E	ED[%]
Adc	R8	25.9	Adc	R8	25.9
	R7	24.4		R7	24.4
fc	R2	45.7	fc	R2	45.7
	R3	19.5		R3	19.5
	C1	9.32		C1	9.32
A1	R4	11.8	A1	R4	11.8
	C2	14.6		C3	14.6
A2	R9,C5	14.5	A2	R9,C5	14.5
A3	R5	113	A3	R5	113
	C3	41.7		C3	41.7
	R4	31.3		R4	31.3
A4	R6	56.1	A4	R6	56.1
A5	R1	49.6	A5	R1	49.6

The Chebychev filter is composed of three blocks. Even when we have access to the output of analog block, some element cannot be tested accurately. This is the case of the element R5. In fact, a deviation less than 113% in R5 may not be tested if the worst case is considered (Table 3). Note that, in case 2, when the output of the third block of the chebychev filter is connected to the conversion block, the element are tested by the same accuracy as in case 1.

For the digital block, the results obtained for some benchmark circuits are shown in Table 4. This table shows, for each circuit, the number of primary inputs (#PI), number of primary outputs(PO), the number of collapsed faults. It shows also, for each circuit, the number of untestable faults, number of vectors and the CPU time in both cases (with and without constraints).

The constraints are imposed by the conversion block composed of 15 comparators and 15 reference voltages.

Table 4: Test vector Generation, with and without constraints, for some benchmark circuits

Circuit	#PI	#PO	Collap. Faults	Without constraints			With constraints		
				#Untestable Faults	#vect.	CPU [s]	#Untestable Faults	#Vect	CPU [s]
c432	36	7	524	4	52	220	11	56	937
c499	41	32	758	8	56	318	8	65	1230
c880	60	26	942	0	71	10	12	63	61
c1355	41	32	1574	8	89	680	12	104	1574
c1908	33	25	1979	9	138	1025	81	119	2200

According to Table 4, when constraints are added to the test vector generator, we note that the fault coverage and the time spent for test vector generation are affected. An increase in the number of untestable faults is noted for all the circuits but C499. In the first case, when we have no constraints on the PIs of a circuit, a random test vector generator can be used to accelerate test vector generation. In the second case, a random test pattern can be simulated only if it satisfies the constraints imposed by the analog block of the mixed circuit. For, this reason we have chosen to generate all the test vectors deterministically.

Table 5: Propagation of faulty parameters through comparators

Circuit	#PIs	#PIs from fault (deviation less than x%) cannot be propagated	#PIs through which an analog fault (deviation greater than x%) cannot be propagated.	CPU
c432	36	15	1	150
c499	41	15	4	41.2
c880	60	15	1	3.5
c1355	41	15	2	58.3
c1908	33	15	1	39.5

Now let us see at which comparator analog faults can be activated and propagated. To test if the deviation on a parameter exceeds its tolerance or not, the amplitude and a frequency of the analog signal is chosen according to Table 1. Since the amplitude depends on a reference voltage, and there are 15 comparators in the conversion block, the fault can be observed at the 15 POs of the comparators. In this table, we have studied the case when only one primary output of the conversion block behaves differently in a faulty and in a fault-free circuit. It is shown in Table 5 that, for the circuit C499, if a deviation in the amplitude is less than -5%, then analog faults cannot be propagated through 4 comparators. This means that the reference voltages connected to those comparators cannot be tested. Then, all the reference voltages should be tested in order to have the best coverage of all the resistors of this block. Note also, that for the same circuit, any deviation greater than 5% in the gain can be propagated through any comparator to a primary output.

Table 6: Conversion-circuit element coverage when its input and outputs are directly accessed

T	Vt1	Vt2	Vt3	Vt4	Vt5	Vt6	Vt7	Vt8	Vt9	Vt10	Vt11	Vt12	Vt13	Vt14	Vt15
E	R1	R2	R3	R4	R5	R6	R7	R8,R9	R10	R11	R12	R13	R14	R15	R16
ED [%]	15	31	41	51	62	71	81	91	77	64	52	40	29	17	6

Table 6 gives the results of the conversion-block-elements testing in case 1, whereas Table 7 gives the results for the conversion-block-element testing in case 2.

According to Table 6, R5 can be tested for a deviation of 62% when the conversion-block inputs and outputs can be directly accessed. But in case 2, due to the dependencies between digital inputs, when the digital block is the c432 circuit, R5 is tested by a deviation greater than 71%, in the worst case, through the comparator connected to Vt6 (Table 7).

Table 6 shows the element deviation that can be tested when the digital block is one of the following benchmark circuits: c432, c499, or c1355. The dashed cells in Table 7 tells us that the reference voltage cannot be tested.

**Table 7:** Conversion-block element coverage when it is a part of a mixed circuit.

Comparators connected to c432															
<i>T</i>	Vt1	Vt2	Vt3	Vt4	Vt5	Vt6	Vt7	Vt8	Vt9	Vt10	Vt11	Vt12	Vt13	Vt14	Vt15
<i>E</i>	R1	R2	R3	R4		R6,R5	R7	R8,R9	R10	R11	R12	R13	R14	R15	R16
<i>ED</i> [%]	15	31	41	51		71	81	91	77	64	52	40	29	17	6
Comparators connected to c499															
<i>E</i>		R1, R2	R3	R4		R6, R5	R7	R8,R9	R1, R11		R12	R13	R14	R15,R16	
<i>ED</i> [%]		31	41	51		71	81	91	77		52	40	29	17	
Comparators connected to c1355															
<i>E</i>	Vt1	R2	R3	R4	R5		R7, R6	R8,R9	R10	R11	R12	R13	R14	R15,R16	
<i>ED</i> [%]	15	31	41	51	62		81	91	77	64	52	40	29	17	

### 3.1 Result validation

To validate the proposed technique, a discrete realization of an *analog-digital* circuit is performed. The analog circuit is the state variable filter, the digital circuit is a 4-bit adder and the conversion circuit is an 8-bit A/D converter, Figure 8. The experimental results are shown for every block considered as alone and when they are a part of a mixed circuit. With an incremental sensitivity analysis and the computation of the worst case component deviation, we found that to guarantee the maximum coverage of all the components, the performances  $\{A1_{dc}, A2_{dc}, A3_{dc}, A3'_{dc}, A1_{10kHz}, A2_{10kHz}, f_{h1}\}$  should be measured. These performances are selected among  $\{A1_{dc}, A2_{dc}, A3_{dc}, A3'_{dc}, A_{max1}, A_{max2}, A_{max3}, A1_{10kHz}, A2_{10kHz}, A3_{10kHz}, f1, f2, f3, f_{h1}, f_{h2}, f_{h3}, f_{l1}, f_{l2}, f_{l3}\}$  where:

$A1_{dc}$ : DC gain computed at output  $V_i$ , for  $i=1$  to 3.

$A3'_{dc}$ : DC gain computed at output  $V3$  when  $V_{in}$  is below a threshold voltage

$A1_{max}$ : Maximum AC gain computed at output  $V_i$ , for  $i=1$  to 3.

$f_i$ : frequency of the maximum AC gain computed at output  $V_i$ , for  $i=1$  to 3.

$f_{li}$ : Low cut-off frequency computed at output  $V_i$ , for  $i=1$  to 3.

$f_{hi}$ : High cut-off frequency computed at output  $V_i$ , for  $i=1$  to 3.

Some experimental results are provided for the state variable filter using discrete components realization. The output signal of the non-faulty filter is firstly measured, then, a fault is injected in the filter and the output signal is observed. The values of the faults (component deviations) are given in Table 8. In this experiment, we suppose that we have only one faulty element. All the possible faults were injected, and we found that the computed worst case component deviation forces the measured performance deviation (MPD) to be out of its tolerance box  $([-5\%, +5\%])$ .

We have found that a fault which is even less than the computed component deviation (CD) can be detected, Table 8. This means that our computation is very pessimistic since we consider the worst case, and this does not occur frequently. Then, we have observed that every fault greater than the CD is easily detected at the output of the digital block.

**Table 8:** Test results for the state variable filter.

<i>T</i>	<i>C</i>	<i>CD</i> [%]	<i>MPD</i> [%]
$A1_{dc}$	R3	21	13
	R1	13	9.1
$A2_{dc}$	R2	8	5
	R6	20	5.5
$A3$	R7	21	6.5
	R4	23	21
$A3'_{dc}$	R5	23	28
	R9	24.5	44
$A1$	C2	24.5	31
	R8	26	50
$A2$	C1	26	33
	R	20	14

Table 8 shows the performances to be measured (*T*), components (*C*), the deviation at which they are tested (*CD*) and the measured parameter deviation (*MPD*). It is obvious that all the

component deviations can be detected, since this deviation forces the measured parameter to be out of its tolerance box. The components are tested with the same accuracy when the analog circuit is considered alone and when it is a part of the mixed circuit of Figure 8. This is the fact that all the considered faults can be propagated through the digital circuit. For the digital circuit, we have injected faults (stuck-at 0 and stuck-at 1) at the inputs of the 4-bit adder.

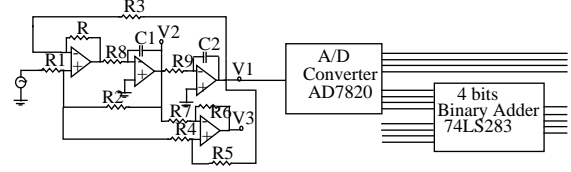


Figure 8: A mixed circuit composed of a state variable filter, A/D converter and a 4-bit adder

### 4. Conclusion

In this paper we have proved that a mixed circuit can be tested as entity without modification. The analog inputs can be easily activated and the fault can be propagated through the digital block using an algebraic method based on BDDs. For digital circuit testing, the current implementation uses the single stuck-at fault model. The dependency introduced by the connection of the blocks (digital, analog and conversion) makes test vector generation harder for test generators based on gate-level representation. We used an algebraic method based on OBDD representation that allows us to efficiently manipulate boolean functions. The constraints imposed by the analog block are taken into account during test vector generation. Simulation results as well as the practical validation confirm the efficiency of the proposed method.

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